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FPGA IMPLEMENTATION OF 3GPP-LTE PHYSICAL DOWNLINK ...
FPGA IMPLEMENTATION OF 3GPP-LTE PHYSICAL DOWNLINK CONTROL CHANNEL USING DIVERSITY TECHNIQUES S SYED AMEER ABBAS #1, S J THIRUVENGADAM #2 # Department of Electronics and Communication Engineering 1 Mepco Schlenk Engineering College, Sivakasi-626005, INDIA 2 Thiagarajar College of Engineering, Madurai- 625015, INDIA 1 abbas_mepco

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FPGA Prototyping of A High Data Rate LTE Uplink Baseband ...
implementation Hence, the system architecture should be well designed to achieve high data rate and good error-rate performance This paper presents an architecture and an FPGA prototype of an LTE uplink MIMO receiver This work, to the best of the author’s knowledge, is the first FPGA prototype of the LTE

Automated performance-based design technique for an ...
developed to design SoC on a heterogeneous FPGA-CPU platform on the basis of performance metrics such as area, power, and latency Design of physical downlink shared channel (PDSCH) in long-term evolution (LTE) is presented as a case study This paper provides the implementation of the

transmitter

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Software Defined Radio Implementation of LTE Transmitter

paper presents a Field Programmable Gate Array (FPGA) design and implementation of the transmitter of the LTE downlink physical layer according to releases 8 and 9 on Virtex 6 XC6VLX240T FPGA kit using Xilinx® ISE® Design Suite version 121 General Terms SDR, LTE, 4G, 3GPP, OFDM, Transmitter , 2G ,3G, LTE

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Oct 11, 2020 · Fpga Implementation Of An Lte Here's a review of the LTE algorithms and a practical implementation on a Xilinx FPGA The reference design is tested using multiple video stream with varying encoding rates By Rob Payne, Xilinx dspdesignlinecom (February 06,

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The Application of FPGAs for Wireless Base-Station ...

with base station connectivity, the implementation of these functions in Xilinx FPGA technology, and the expected resource and device-mapping re quirements for several example applications The practical goal is to provide an overview of how wireless base station connectivity applications can

AN503: Implementing OFDM Modulation for Wireless ...

wireless systems, including WLAN, WiMAX, and 3GPP LTE systems A straightforward implementation of OF DM modulation in multiple-input multiple-output (MIMO) systems is to duplicate the data path, including the FFT core for every antenna A more resource-friendly solution is to share the FFT core among antennas FFT reuse for MIMO requires that the

FPGA Implementation of LTE Downlink Transceiver with ...

paper presents a Field Programmable Gate Array (FPGA) design and implementation of the LTE downlink transmitter and receiver according to releases 8 and 9 on Virtex 6

1.5 Gbit/s FPGA Implementation of a Fully-Parallel Turbo ...

Field-Programmable Gate Array (FPGA) implementa-tions We propose a model FPGA implementation When using a Stratix IV FPGA, the proposed FPTD FPGA implementation achieves an average throughput of 153 Gbit/s and an average latency of 056 s, when decoding frames comprising N=720 bits These are respectively 132

IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING ...

our VLSI architecture Section V provides reference FPGA implementation results and a trade-off analysis We conclude in Section VI All proofs are relegated to the Appendices II LARGE-SCALE MIMO IN LTE UPLINK We next introduce the LTE uplink model and present a new and efficient method for linear soft-output minimum mean-

DIFFERENT FPGA PRODUCTS BASED IMPLEMENTATION OF ...

Abstract- In the long- term evolution(LTE) physical layer, using turbo code is considered the core of the error-correcting code This paper presents an implementation of LTE turbo decoding using the Log- Maximum a posteriori (MAP) algorithm with reduced number of required cycles approximately by 75% based on serial to parallel operation

Design and FPGA Implementation of an OFDM System Based ...

Entitled: “Design and FPGA Implementation of an OFDM System Based on 3GPP LTE Standard over Multipath Fading Channel” and submitted in partial fulfillment of the requirements for the degree of Master of Applied Science Complies with the regulations of this University and meets the accepted standards with respect to originality and quality

LabVIEW Communications LTE Application Framework 19.5 ...

LTE FPGA USRP RIO 120 MHz BW eNodeBgvi o UE o Provides the UE side in a double-device setup o Implements the DL RX and the UL TX of a UE including the basic UE MAC functionalities (refer to the lower part of Figure 19) o Top-level host VI: LTE Host UEgvi o The top-level FPGA VI is one of the following VIs: LTE FPGA FlexRIO UEgvi LTE FPGA

FPGA IMPLEMENTATION OF A REALTIME CYCLOSTATIONARY ...

FPGA IMPLEMENTATION OF A REALTIME CYCLOSTATIONARY FEATURE DETECTOR FOR OFDM SIGNALS Sean Hamlin Follow this and additional works at:https://digitalrepositoryunmedu/ece_etds hotspots, and the advent of LTE-A Along with the incumbent spectrum users for LMR, TV, radio, avionics and military communications, the ability to service all users

LogiCORE™ IP LTE RACH Detector v1 - Xilinx

functionality of the application Before implementing the LTE RACH Detector core, it is highly recommended that the designer gain knowledge of the LTE standard, in particular its definition of the Random Access Channel For best results, previous experience building high performance, pipelined FPGA designs using Xilinx implementation

Low complexity MMSE interference cancellation for LTE ...

are not suitable for SDR implementation In order to perform the interference cancellation in a more efficient way, in this paper, we propose a low complexity interference cancellation scheme based on the MMSE criterion to improve the performance of LTE/LTE-Advanced uplink receiver Different from other schemes, our inter-symbol and